

1 **What is claimed is:**

2 1. A sampling circuit for an analog signal
3 according to a clock signal, comprising:

4 a first thin film transistor (TFT), having a first
5 electrode to receive the analog signal, a
6 control electrode to receive the clock signal
7 and a second electrode for sampling the analog
8 signal when the clock signal is at a first
9 logic level; and

10 a counteracting device coupled to the second
11 electrode, wherein when the clock signal is
12 changed from the first logic level to a second
13 logic level, feed-through voltage drop caused
14 by a parasitic capacitor between the second
15 electrode and the control electrode of the
16 first TFT is reduced.

1 2. The circuit as claimed in claim 1, wherein the
2 counteracting device is a capacitor between the second
3 electrode and a reference potential node.

1 3. The circuit as claimed in claim 1, wherein the
2 counteracting device comprises an inversion device,
3 having an input terminal coupled to the control
4 electrode, and a capacitor between the second electrode
5 and an output terminal of the inversion device.

1 4. The circuit as claimed in claim 3, wherein the
2 capacitor comprises a second TFT having a gate terminal
3 coupled to the output terminal of the inversion device

4 and a source and drain terminal both coupled to the
5 second electrode.

1 5. A liquid crystal display, comprising:
2 a plurality of display units, arranged in array;
3 a plurality of data lines disposed corresponding to
4 each line of the display units, wherein each
5 data line provides a video signal to the
6 corresponding display unit; and
7 a data driving circuit, having at least one
8 sampling circuit, sampling an image signal to
9 be the video signal according to a clock
10 signal, and the sampling circuit comprising:
11 a first thin film transistor (TFT), having a
12 first electrode receiving an analog
13 signal, a control electrode receiving the
14 clock signal, and a second electrode for
15 sampling the analog signal when the clock
16 signal is at a first logic level; and
17 a counteracting device coupled to the second
18 electrode, wherein when the clock signal
19 is changed from the first logic level to a
20 second logic level, a feed-through voltage
21 drop caused by a parasitic capacitor
22 between the second electrode and the
23 control electrode of the first TFT is
24 reduced.

1 6. The liquid crystal display as claimed in claim
2 5, wherein the counteracting device is a capacitor

3 between the second electrode and a reference potential
4 node.

1 7. The liquid crystal display as claimed in claim
2 5, wherein the counteracting device comprises an
3 inversion device, whose input terminal is coupled to the
4 control electrode, and a capacitor between the second
5 electrode and an output terminal of the inversion device.

1 8. The liquid crystal display as claimed in claim
2 7, wherein the capacitor comprises a second TFT having a
3 gate terminal coupled to the output terminal of the
4 inversion device and a source and drain terminal, both
5 coupled to the second electrode.